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To: Examiner Sheila Clark
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Re: Proposed Amendments/Interview Agenda
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From: Thomas E. Brown

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35 U.S.C. §112, Second Paragraph Rejection

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With regard to the rejection of claims 4 and 5 under 35 U.S.C. §112, second paragraph, we propose to amend claims 4 and 5, as attached herewith, to overcome this rejection.

As to the Merits

Claim 1 calls for wires provided in a first layer . . . and wire dummies provided in a second layer different from the first layer by avoiding areas that are directly above or below positions of said wires provided in said first layer.

For example, as shown in FIG. 2 of the present invention, wire dummies 13 of the Nth layer are not placed in areas that are directly above or below the positions of wires 11, 12 of the N+1th layer or wires 14, 15 of the N+1th layer, respectively.

In FIG. 7 of Ushiku, the upper-layer patterns 202, 203 and 204 are positioned directly above the dummy patterns 30a-30c and 40. Thus, Ushiku fails to disclose the features of claim 1.

With regard to Bothra, in FIG 2B Bothra discloses that the signal wires 216 and the wire dummies 226 are provided in the same layer. That is, Bothra fails to disclose a wire dummies provided in a second layer different from the first layer by avoiding areas that are directly above or below positions of said wires provided in said first layer, as called for in claim 1.

Claim Amendments

Claim 4 (Currently Amended): A semiconductor integrated circuit, comprising:

a plurality of layers provided on a semiconductor substrate;

signal wires and power supply lines are provided in a first layer that is one of said plurality of layers; and

wire dummies provided in a second layer different from the first layer and having an arrangement that avoids areas overlapping positions of said signal wires,

~~wherein said wires are signal wires excluding power supply wires, and~~

said wire dummies are further provided in areas overlapping positions of said power supply wires that are provided in the first layer.

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Claim 5 (Currently Amended): A semiconductor integrated circuit, comprising:
a plurality of layers provided on a semiconductor substrate;
signal wires and power supply wires are provided in a first layer that is one of said plurality of layers; and
wire dummies provided in a second layer different from the first layer and having an arrangement that avoids areas overlapping positions of said signal wires,
~~wherein said wires are signal wires excluding power supply wires.~~
said wire dummies are further provided in areas overlapping positions of said power supply wires that are provided in the first layer, and
said signal wires have a width less than a predetermined wire width, and said power supply wires have a width greater than the predetermined wire width.

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